



SHEET 1 OF 2

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APPLICANT(S): Chan et al.

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U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
RL	A1	5,467,883	11/21/95	Frye et al.	216	60	11/27/93
	A2	5,559,690	9/24/96	Keeler et al.	364	164	9/16/94
	A3	5,654,903	8/5/97	Reitman et al.	364	551.01	11/7/95
	A4	5,740,033	4/14/98	Wassick et al.	364	149	10/13/92
	A5	6,268,226	7/31/01	Angell et al.	438	16	6/30/99

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
RL	B1	WO 01/57605	8/9/01	WO	G05B	13/04	1/11/01	N	Y
RL	B2	DE196 37 917 A1	3/19/98	DE	G05B	13/04	9/17/96	Y	

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
RL	C1	Card et al., "Dynamic Neural Control for Plasma Etch Process," <u>IEEE Transactions on Neural Networks</u> , (1997).
	C2	Dillon et al., "Guest Editorial Everyday Applications of Neural Networks," <u>IEEE Transactions on Neural Networks</u> , 8:4 (1997).
	C3	Hatzipantelis et al., "Comparing Hidden Markov Models with Artificial Neural Network Architectures for Condition Monitoring Applications," <u>Artificial Neural Networks</u> , 26-28, Conference Publication No. 409 (June 1995).
	C4	Kim et al., "Intelligent Control of Via Formation by Photosensitive BCB for MCM-L/D Applications," <u>IEEE Transactions on Semiconductor Manufacturing</u> , 12:503 (1999).
	C5	Konstantopoulos et al., "Controllers with Diagnostic Capabilities. A Neural Network Implementation. Journal of Intelligent and Robotic Systems," Department of Electrical Engineering, University of Notre Dame, IN 12: 197-228 (1995).



C6	Moyné, "AEC/ APC Vision: A Research and Suppliers' Point of View," 3 rd Annual European AEC/APC Conference Proceedings (2002).
C7	Rietman et al., "A Study on $\mathcal{R}^m \rightarrow \mathcal{R}^1$ Maps: Application to a 0.16- μ m Via Etch Process Endpoint," <u>IEEE</u> (2000).
C8	Rietman et al., "A System Model for Feedback Control and Analysis of Yield: A Multistep Process Model of Effective Gate Length, Poly Line Width, and IV Parameters", <u>IEEE</u> (2001).
C9	Rietman, "Neural Networks in Plasma Processing," <u>Journal of Vacuum Science and Technology: Part B, IEEE Transactions on Semiconductor Manufacturing</u> , 14:1 (2001).
C10	Smyth et. al., "Hidden Markov Models an Neural Networks for Fault detection in Dynamic Systems," California Institute of Technology (1993).
C11	Zhang et al, "Control of Spatial Uniformity in Microelectronics Manufacturing: An Integrated Approach," Proceedings of AEC/APC (2000).
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DATE CONSIDERED	2/8/05